REMARKS/ARGUMENTS

Prior to this amendment, claims 1-35 were pending. In this amendment, claims 34 and 35 are amended, and no claims are canceled or added. No new matter is added. Thus, after entry of this amendment, claims 1-35 will remain pending.

Interview

Applicants would like to thank the Examiner for extending the courtesy of a telephone interview with counsel, David B. Raczkowski, on April 15, 2009. Clarification of the disclosures of Calhoun and Yu were discussed. Specifically, that Calhoun does not provide the claimed first mode, and that Yu does not provide motivation to convert an N-bit number to a 2N-bit number at an input of the 2N-bit multiplier used also for the second mode, were discussed.

Claim Rejections – 35 USC § 112, Second Paragraph, indefiniteness

Claims 34 and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite and unclear. Claims 34 and 35 have been amended to correct the typographical errors pointed out by the Examiner.

Claim Rejections – 35 USC § 103(a), Moyse, Callhoun, Yu, Langhammer

Claims 1-6, 11-19, 24-27, and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moyse (US Pat. 5,446,651) in view of Calhoun et al. (hereafter Calhoun)(US Pat. 3,752,971) Yu (6,523,055) and Langhammer et al. (hereafter Langhammer)(US Pat. 6,693,455).

Claim 1

Claim 1 is allowable over these cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1. For example, claim 1 recites:

> *in the first mode for multiplying two N-bit numbers,*
> *a first long word length multiplicand is formed at the first 2N-bit input from a first short word length multiplicand stored in the first register,*
> *a second long word length multiplicand is formed at the second 2N-bit input from a second short word length multiplicand stored in the second register, and*

the first and second long word length multiplicands are multiplied together using the 2N-bit multiplier to form a 4N-bit result that includes the product of the first and second short word length multiplicands.

A. Moyse and Calhoun both teach the same operation

Moyse is cited for teaching the claimed second mode. The Office Action acknowledges that Moyse does not teach the claimed first mode, but asserts that Calhoun does. However, Calhoun just teaches the 2N by 2N multiplication mode (asserted second mode) of Moyse, which multiplies two 2N-bit numbers to create a 4N-bit product. *See Calhoun*, col. 8 lines 15-18. For example, Calhoun uses four N-bit multipliers as a 2N-bit multiplier, which provides the 4N-bit final product from an input of two 2N-bit numbers. *Id.*, FIG. 4 and col. 2 lines 52 to col. 3 line 5. Thus, Calhoun does not teach the claimed first mode for multiplying two N-bit numbers using a 2N-bit multiplier.

B. Yu teaches sign or zero extending after multiplication, not at an input

The Office Action asserts that Yu discloses forming a 2N-bit multiplicand by sign or zero extending an N-bit multiplicand at an input of a multiplier. However, Yu performs the sign extending after multiplication, i.e. extending the product of the multiplication. *See Yu*, col. 11 lines 32-36 and col. 14 lines 14-20. Since Yu performs the extending after multiplication, Yu does not provide a sign or zero extended 2N bit number at an input of a multiplier.

Accordingly, Moyse and Calhoun in combination with Yu do not teach or suggest "*a first long word length multiplicand is formed at the first 2N-bit input from a first short word length multiplicand stored in the first register*," as recited in claim 1.

Additionally, the Office Action states "extending would allow for multiplication to be performed in any sized multiplier." Such a motivation is not provided anywhere in Yu, and is improper hindsight. Such motivation is obtained from knowledge only gleaned from the present application and not from other knowledge which was within the level of ordinary skill in the art at the time the claimed invention was made. *See MPEP* § 2145 X.A.

C. The claimed accumulation units have not been identified

The Office Action asserts that Langhammer, at FIG. 5 and col. 7 lines 24-49, teaches "*a first and a second 2N-bit accumulation unit, each having an input connected to an*

output of the 2N-bit multiplier." However, the Office Action has not provided an identification of which two adders 41 of Langhammer correspond to the claimed accumulation units and which multiplier 13 is asserted to be the claimed 2N-bit multiplier.

Accordingly, Applicants request identification of which of the adders 41 of FIGS. 5 or 6 are asserted to be the claimed two 2N-bit accumulation units and which multiplier 13 is asserted to be the claimed 2N-bit multiplier.

For at least these reasons, claim 1 and its dependent claims are allowable over the cited references.

Claims 14 and 26

Applicants submit that independent claims 14 and 26 and their respective dependent claims are allowable for a same reason as claim 1

Allowable Subject Matter

Applicant would like to thank the Examiner for the indicated allowability of claims 34 and 35 if rewritten to overcome the rejections under 35 USC § 112, second paragraph, set forth above, and to include all of the limitations of the base claim and any intervening claims.

In view of the foregoing arguments with regard to claims 1, 14 and 26, Applicant respectfully submits that claims 34 and 35 are in condition for allowance without being rewritten in independent form.

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CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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